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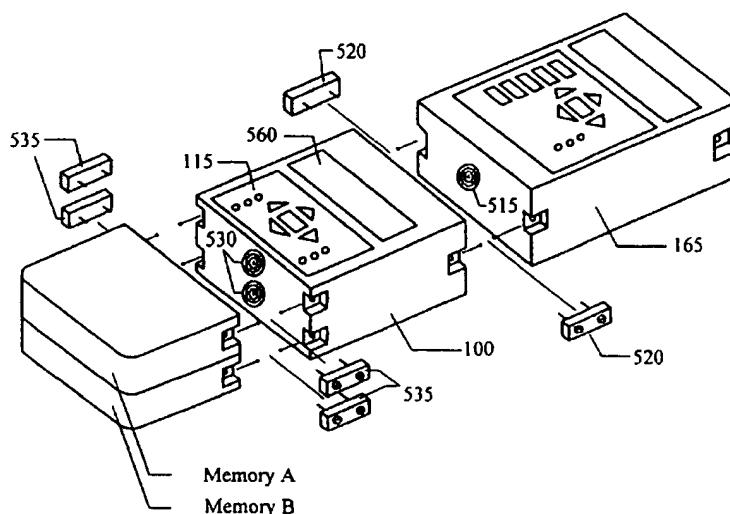
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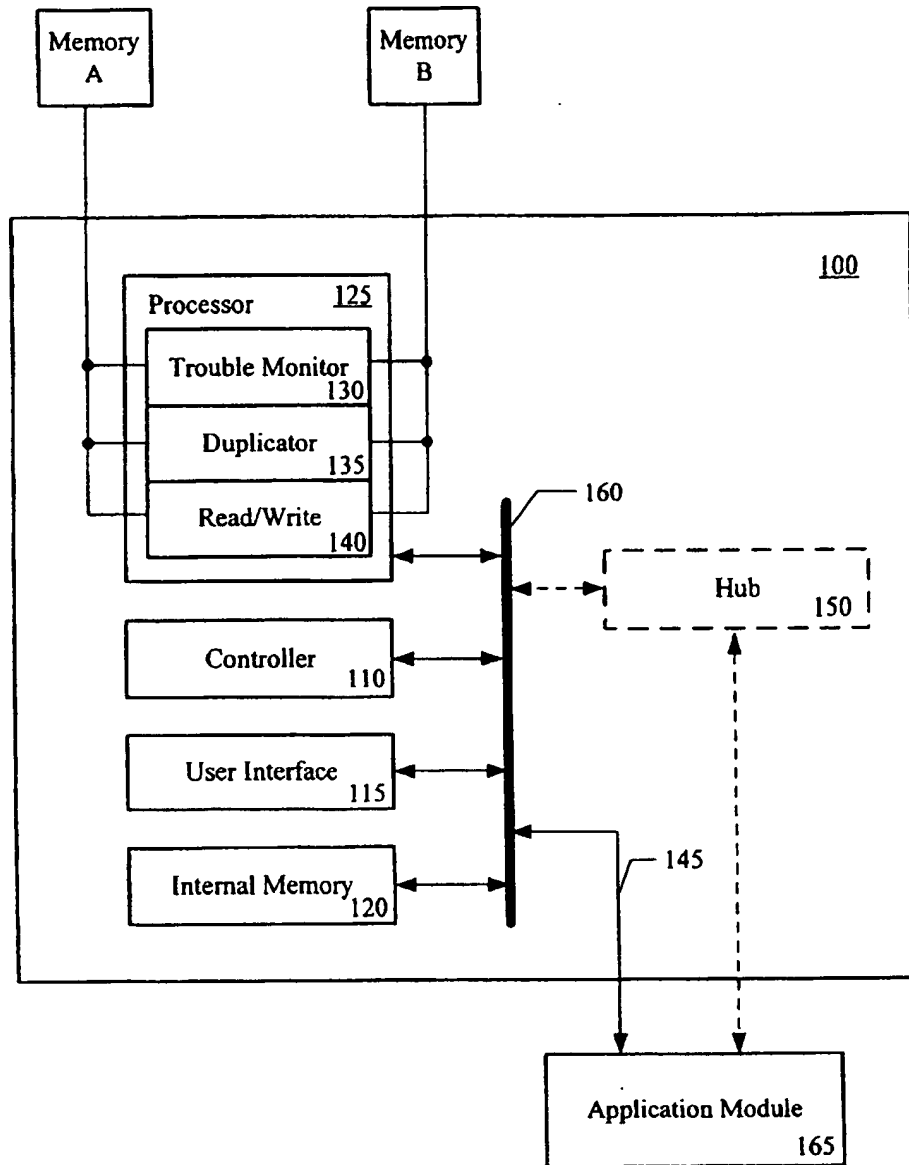
(54) Abstract Title: **Master slave data management system**

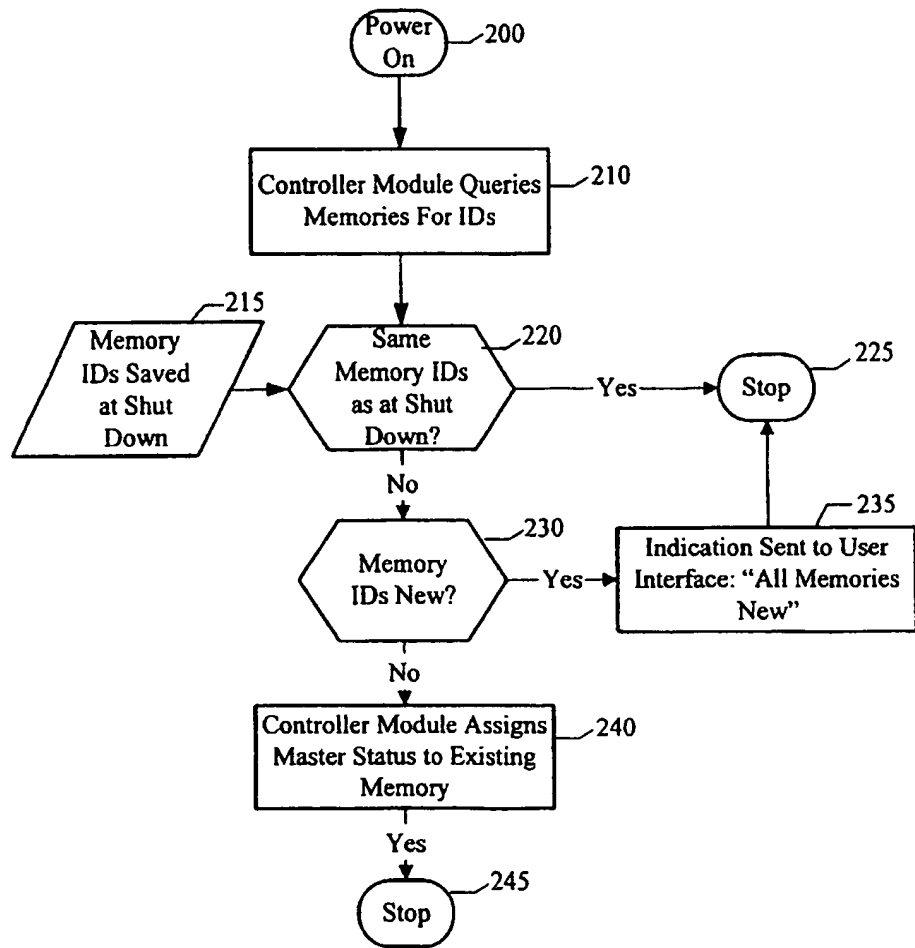
(57) A master-slave data management system includes a bus (160) in communication with a processor (125), a first data path separate from the bus (160) providing the processor (125) with communication to a first memory (memory A), and a second data path separate from the bus providing the processor (125) with communication to a second memory (memory B). The processor (125) is configured to form a redundant array of independent memories by establishing the first memory (memory A) as a master memory and subsequently writing to the second memory (memory B) to make the second memory (memory B) a slave memory.

The system can be used to back up memory in portable MP3 players and digital cameras, for example.



### Figure 5

**Figure 1**

**Figure 2**

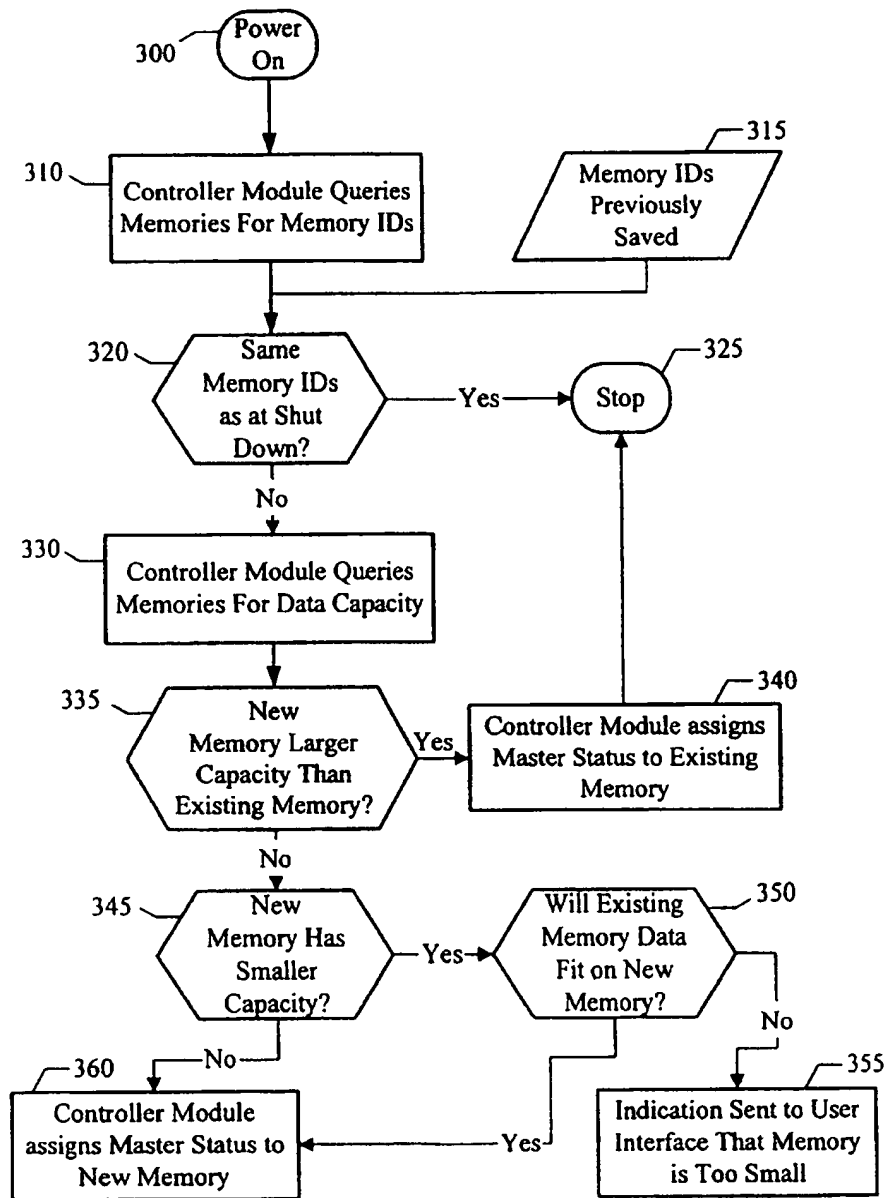
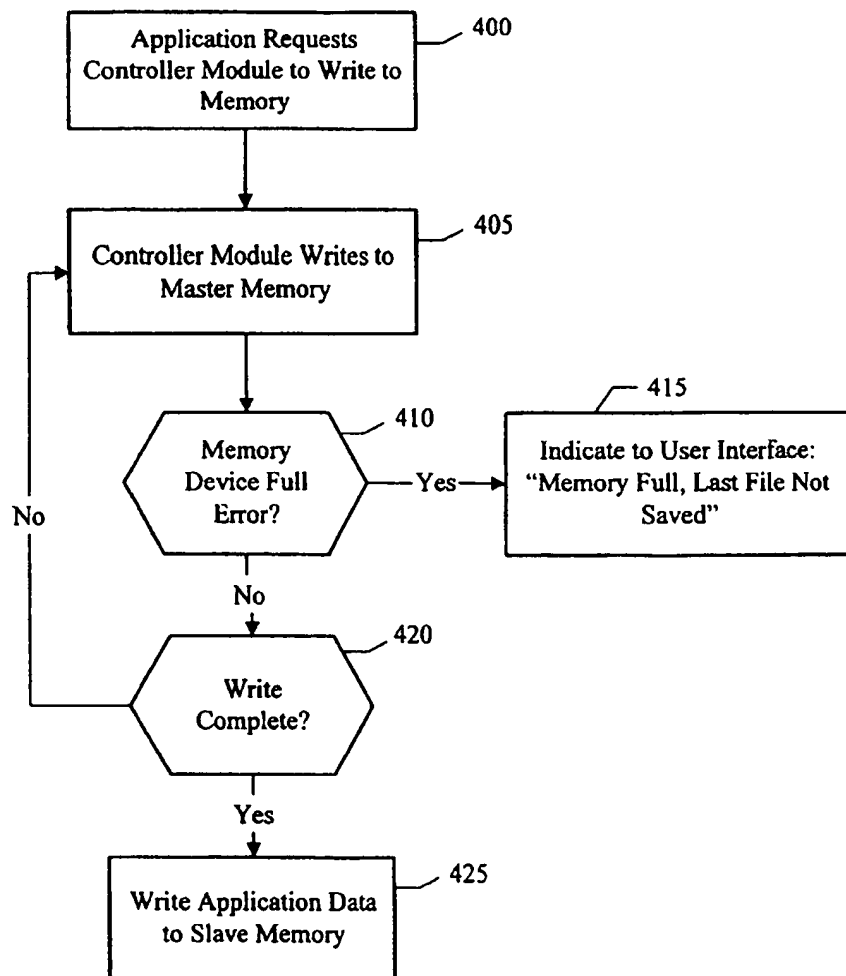
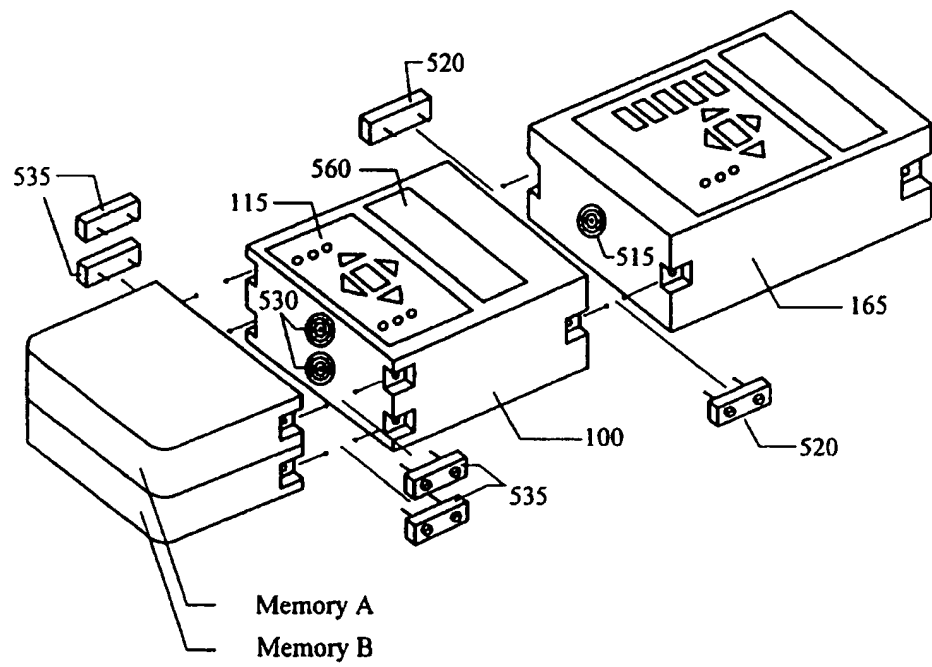
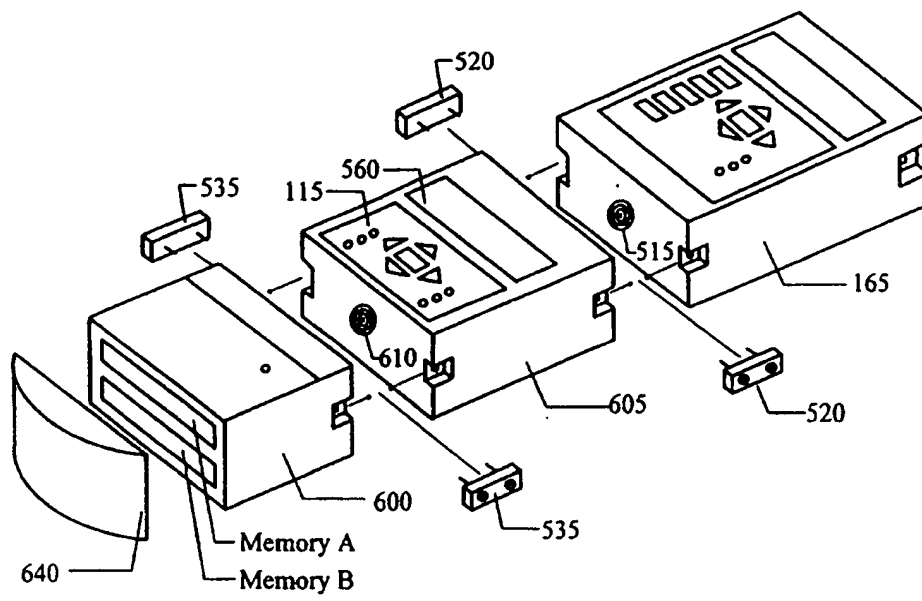
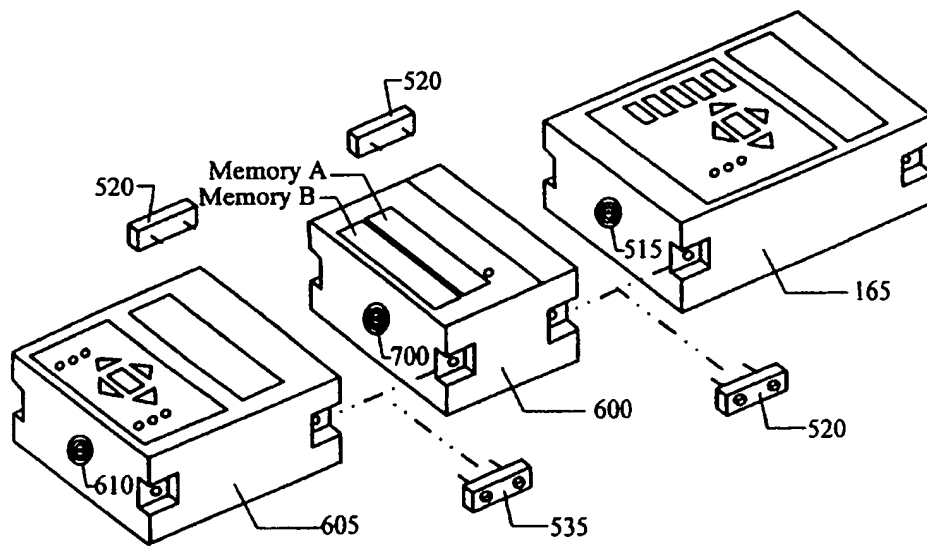


Figure 3

**Figure 4**

**Figure 5**

**Figure 6**

**Figure 7**



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**MASTER-SLAVE DATA MANAGEMENT SYSTEM AND METHOD**

BACKGROUND OF THE INVENTION

**[0001]**     Field of the Invention

**[0002]**     This invention relates to electronic systems,  
5 and more particularly to master-slave data management  
systems and methods.

**[0003]**     Description of the Related Art

**[0004]**     Electronic devices manufactured for capturing,  
10 creating, storing, manipulating or transferring digital  
music, sound, images, movies or other encoded data are  
more prevalent with the advent of inexpensive semiconduc-  
tor processing and increased consumer demand. Products  
such as portable MP3 (Moving Picture Experts Group Layer  
15 3 Standard) players, digital cameras and digital voice  
recorders continue to gain popularity. The general trend  
for each of these commercial devices is to provide for  
greater data storage capability at reduced cost.

**[0005]**     Unfortunately, the trend for providing greater  
20 memory in these devices is accompanied with the trend in  
increased cost and time wasted when such large amount of  
data is lost from a memory device failure. Many portable  
electronic devices lack redundancy in design; such lack  
fails to help the consumer recover from a memory device  
25 failure. Even for devices that have the ability to pro-

vide back-up data, time spent restoring previously backed-up data is tedious and troublesome for the average consumer. Also, should a purchaser desire to upgrade a memory device in their product, a time-consuming process  
5 ensues with the purchaser often using a PC to back up data for restoration onto the replacement memory device.

[0006] Some manufacturers have attempted to solve these problems through increased data throughput to PCs for backup and file transfer. Unfortunately, the single  
10 memories in these devices often fail prior to back-up due to physical shock such as dropping, or normal wear and tear. Another solution utilizes two banks of DIMMS (dual in-line memory modules). In this solution, data is written to a first bank at the same time a second bank is  
15 reading data for the next write. If one bank fails, the data is written from the bank that mirrors the data to replace the failed memory. Another approach includes a RAID (redundant array of industry-standard DIMMS) memory solution using five memory controllers to control five  
20 memory banks of industry-standard DIMMS. The memory controllers split the data into four blocks and write the four blocks to the four memory banks. A RAID processor calculates parity information which is stored on the fifth memory bank. If any one of the memory banks requires replacement, the data can be recovered from the  
25 remaining four memory banks. Each of these solutions provides for data redundancy, but the solutions do not provide mechanisms for consumer-friendly memory repair and upgrade in portable devices.

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#### SUMMARY OF THE INVENTION

[0007] Therefore, there still exists a need for a portable electronic device system that provides for data redundancy without the use of a PC, and that may provide for easy memory upgrade capability without the use of a PC in the transfer. One embodiment of the present invention is described by a system including a bus in communication with a processor, a first data path separate from the bus providing the processor with communication to a first memory, and a second data path separate from the bus providing the processor with communication to a second memory, wherein the processor is configured to form a redundant array of independent memories by establishing the first memory as a master memory and subsequently writing to the second memory to make the second memory a slave memory.

[0008] Also, an embodiment of the invention is described as including a controller module in communication with a master memory and a slave memory through first and second independent data paths, respectively, and an application module in communication with the controller module. The application module sends application data to the controller module and the controller module sends the application data first to the master memory and then sends the application data to the slave memory.

[0009] A method is described for distinguishing between existing and new memories by receiving a first current memory identification ("ID") representing a first memory, receiving a second current memory ID representing a second memory, and comparing each of the first and second current memory IDs to previously saved first and second memory IDs.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principals of the invention. Moreover, in the figures, like reference numerals designate corresponding parts throughout the different views.

[0011] Figure 1 is a block diagram of an embodiment of a system of redundant memory showing the redundant memory in direct connection with a processor.

[0012] Figure 2 is an embodiment a flow diagram for assigning master status to a memory using memory IDs in the system shown in Figure 1.

[0013] Figure 3 is an embodiment of a flow diagram for assigning master status to a memory using application data capacity in the system shown in Figure 1.

[0014] Figure 4 is a flow diagram illustrating an embodiment of a method for using master status to manage data flow within the system shown in Figure 1.

[0015] Figures 5, 6, and 7 are exploded, perspective views illustrating three different systems of redundant memory utilized in a memory storage at different locations in a portable electronic device.

#### DETAILED DESCRIPTION OF THE INVENTION

[0016] The invention provides a system for managing and storing data in a memory storage module for use with consumer applications such as MP3 players, digital recorders, or any other electronic device enabling the capture, creating, storing, manipulating or transferring of digital music, sounds, images, movies or other encoded data.

Through the use of a plurality of memories, a redundant array of independent memory is available for a controller module and for at least one consumer application. One of the memories is assigned to be a master memory by comparing memory capacities between memories, or through a determination of which memory is new to the system (a "new memory") and which memory remains installed (an "existing memory"). The memory that the new memory replaced is removed from the system ("discarded memory"). By writing to the master memory first and to the slave memory second, a system is created to reduce the effects of data loss through damage to a memory device. An embodiment of the invention also provides for memory upgrades without the use of a personal computer (PC) through management of the write process within the device itself.

[0017] Several embodiments are described in the context of two memories, memories A and B, but may be extended to describe the use of more than two memories. Figure 1 illustrates an implementation scheme for a controller module 100. The controller module 100 is shown in communication with memories A and B and application module 165. The controller module 100 includes a bus 100 in communication with a controller 110, a user interface 115, an internal memory 120, and a processor 125. The various components manage the application data received through the data path 145 for the controller module 100 and manage data from and between memories A and B. The processor 125 and controller 110 may be integrated into a single device. Similarly, internal memory 120 may be integrated onto a single chip with either the processor 125 or controller 110, or both.

[0018] The processor 125 provides several functions including a trouble monitor 130, a duplicator 135 and a read/write circuit 140. The trouble monitor 130 and processor 125 detect whether memories A and B connected to processor 125 are operating correctly and notify the user of problems through the user interface 115. Duplicator 135 enables duplication of application data from memory A to memory B without the use of other external devices such as a PC. The duplicator 135 also communicates through the bus 160 to the user interface 115 to provide information to a user regarding duplication efforts. The read/write circuit 140 communicates with external applications such as an application module 165, and governs the read/write of data to master and slave memories such as memory A or memory B. In an example, the functions (130, 135, 140) may be implemented in firmware or by using a software controlled general purpose DSP (Digital Signal Processor). Also, a third memory or set of memories may be coupled to the processor 125 at the controller module 100. The bus 160 is illustrated with electrically conductive paths between the processor 125, controller 110, user interface 115, and internal memory 120. An optical bus may also be used, as well as any manner of signal conduit, medium, or signaling method.

[0019] Memories A and B are shown in direct communication with processor 125. Memories A and B could also communicate with processor 125 through bus 160, utilizing a data protocol having an addressing scheme managed by the processor 125 and controller 110.

[0020] In an alternative embodiment, a hub 150 is provided in the controller module 100 to enable use of the controller module 100 with user applications. The data path 145 for the controller module 100 extending from the bus 145 would be replaced by the hub 150 in communication with the bus 160. A wireless scheme utilizing Bluetooth™ wireless technology or other wireless scheme could also be provided for a data path substitute between the controller module 100, memories A and B and an application module 165. Also, controller module 100 and application module 165 are described as "modules" for convenience. They may be integrated into a single unit for purposes of the described embodiment.

[0021] Referring to Figure 2, an embodiment of an implementation scheme is illustrated for assigning one of memory A and memory B to be a master memory. The memory that is written to first is referred to as the master. For example, if memory A is assigned master status, then data arriving from the application module 165 through the controller module 100 will be written first to memory A, and then to memory B. The method begins with power on of the controller module 100 (block 200). The controller module 100 uses processor 125 to query memories A and B for their IDs (block 210). The processor 125 retrieves the IDs previously saved at the last shut down (block 215) from the internal memory 120 and compares them to the ID numbers retrieved from the present inquiry (block 220). If the previously saved-and-retrieved IDs match, the process ends (block 225). If both IDs retrieved from the memories are different from the previously saved IDs (blocks 215, 230), an indication is sent by the processor

125 to the user interface 115 that both memory A and B are new (block 235), and the process ends. If only one of the memory IDs are new, then the controller module 100 assigns master status to the existing memory (block 240) using the processor 125, and the process ends (block 245).

[0022] The memory IDs can be serial numbers. Also, although the memory device IDs are saved during the shut-down process for the controller module 100, they may be saved at any time prior to a shut down to provide for an eventual comparison at a controller module 100 power on. The indication sent to the user that both memories are new (block 235) may be replaced with any suitable indication that the process of determining a master memory is as yet undetermined. Also, if preferred by the user, such an indication may not be given at all, but rather used internally by the controller module 100.

[0023] Referring to Figure 3, a scheme is illustrated for assigning master status to either memory A or B using the memory capacity of each of the memories. The controller module 100 is powered on (block 300) and queries memories A and B for their IDs (block 310) using processor 125. The retrieved IDs are compared to the memory IDs previously stored at the previous controller module 100 shut-down (blocks 315, 320). If the retrieved IDs and previously stored IDs are the same, the process is stopped (block 325). The controller module assumes neither memory A nor B are new. If any of the retrieved IDs are not the same as the IDs saved at shut down, the controller module 100 queries each of memories A and B for their



memory device data capacity (block 330). Memory returning a new ID is considered to be the new memory.

[0024] If the new memory has a larger data capacity than the existing memory, the controller module 100 assigns  
5 master status to the existing memory (blocks 335, 340) and the process is stopped (block 325). The existing memory replicates its existing data to the new memory. The process described above ensures that subsequent data  
10 writes will result in application data redundancy in both memories because data is written first to the smaller of the memories (the master memory), and then to the larger memory (slave memory). Once the smallest memory device is full (the master memory), further writes are prevented.

15 [0025] If the new memory has a smaller data capacity than the existing memory (block 345), the processor 125 compares the size of the existing application data (if any) on the existing memory with the capacity of the new memory (block 350). If the existing application data on  
20 the existing memory will not fit on the new memory, the user is provided with an indication that the new memory is too small to provide redundancy between the memories (block 355). If the new memory has the same or greater capacity as the existing memory (block 345), or if the  
25 data on the existing memory will fit on the new memory if the new memory is smaller (block 350), then the controller module 100 assigns master memory status to the new memory (block 360).

[0026] Rather than the controller module 100 querying the  
30 memories for their data capacities (block 330), the processor 125 may be provided with a look-up table of memory

application data capacities, based on ID designation or some similar identification. Also, if a user attempts to replace an existing memory with a new memory having less application data capacity than the pre-existing application data on the existing memory (block 350), the user may be provided with indication or warning of the potential loss of data and insufficient capacity in the new memory for redundancy.

[0027] Figure 4 illustrates an implementation scheme for using the master status of a memory to manage the data flow to memories A and B. The application module 165 requests the controller module 100 to write application data to memories A and B (block 400). The controller module 100 writes first to the master memory using the read/write circuit 140 in processor 125 (block 405). The trouble monitor 130 monitors the write for a memory full error (block 410). If the trouble monitor 130 indicates a write error, indicating the master memory is full, the user interface 115 is provided with a message to the user that the memory is full and the last file was not saved (block 415). If the write to the master memory is complete (block 420), the processor 125 continues to write the application data to the slave memory to provide for data redundancy (block 425). The master memory is either an existing memory or a new memory, with the processor 125 ensuring that data redundancy is maintained between the master and slave memories.

[0028] Rather than the controller module 100 receiving a write request from a particular application such as the application module 165, the controller module 100 may request application data from the application module 165.

In such an implementation, the controller module 100 may then receive the application data to provide to the master memory (block 420).

5     **[0029]** The above described embodiments and implementations are implemented in consumer electronic products such as those shown in Figures 5, 6, and 7. In Figure 5, a controller module 100 is shown aligned for mechanical and electrical connection with application module 165 through electrical connector 515 and mechanical connectors 520. The controller module 100 manages the application data sent from the application module 165 to the memories A and B.

15     **[0030]** The application module 165 in communication with the controller module 100 may be any portable electronic consumer application such as a video/still image player or reviewer, a PDA (electronic personal data assistant), or a digital still or video camera. In an alternative embodiment, the application module 165 may be connected in turn to additional application modules (not shown) through an electrical and mechanical connector similar to electrical connector 515 and mechanical connectors 520. In such a case, the controller module 100 may distinguish between the different application modules utilizing a data addressing scheme.

25     **[0031]** Memories A and B are shown aligned for electrical connection with the controller module 100 through electrical connectors 530 and mechanical connectors 535. In an example, the memories may be rotated and reattached with respect to the controller module 100 through the use of the electrical connectors 530 as described above.

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[0032] The physical shape of memories A and B, the controller module 100 and application module 165 are illustrated as rectangular for convenience. Alternatively, they may be stacked in different configurations. For example, and not by way of limitation, the devices may be stacked end to end to form a cylindrical shape, a square-like shape or some other desirable configuration. In such cases, the electrical connectors (515, 530) and mechanical connectors (520, 535) between the memories A and B, controller module 100, and application module 165 modules may be suitably modified.

[0033] Controller module 100 is shown having a user interface 115 and display 560. The user interface 155 comprises a keypad. In alternative implementations, the user interface 155 may be a microphone for speech recognition, a pressure sensitive touch screen using thin film transistors (TFT), or some similar device or combination of devices for inputting information (not shown). The display 560 is used to provide information to the user of the controller module 100 regarding application data transfer, memory device activities, and data retrieval. Alternatively, the display 560 may be incorporated into the user interface 115 utilizing a TFT screen or some similar device, allowing for both display and receipt of information.

[0034] The embodiments shown in Figures 1-4 may also be implemented as shown in Figure 6. Figure 6 shows memory A and B seated in a memory storage module 600 to facilitate acceptance of standardized form factor memories. In this example, memories A, B are each microdisk drives inserted into the memory storage 600. Alternatively, any

manner of small form factor memories may be utilized in memory storage module 600, including a smartmedia card, memory stick, multimedia card or a miniature card format. Although memory A and memory B are inserted in one end of the memory storage module 600, they may be inserted on different sides of memory storage 600. For example, the memories may be inserted on a top side or bottom side rather than on the end. The memory storage module 600 connects to the controller module 605 through electrical connectors 610 on the controller module 100 and memory storage module 600 (memory storage module 600 side not shown). The memories may be left exposed at their ends, or memory storage cover 640 covers slots for memory A and B to protect them from damage. Alternatively, protection may be provided in a different mechanical configuration such as a pair of individually hinged or otherwise engaging covers for receiving memories, or memories A and B may individually disengage from memory storage module 600 from the exterior positions locating memory A and memory B.

[0035] Referring to Figure 7, the controller module 605, application module 165 and memory storage module 600 are shown in a different configuration with respect to each other. Namely, the memory storage module 600 is connected between the application module 165 and controller module 605 using the electrical connectors (515, 130) and mechanical connectors (120, 135) (labels in Figure 2). Also, in this configuration, access to memory A and memory B is from the top of memory storage module 600 rather than from an end.

1. A master-slave data management system having a bus (160) in communication with a processor (125), a first data path separate from the bus providing the processor (125) with communication to a first memory (memory A),  
5 and a second data path separate from the bus (160) providing the processor (125) with communication to a second memory (memory B), wherein the processor (125) is configured to form a redundant array of independent memories by establishing the first memory (memory A) as a  
10 master memory and subsequently writing to the second memory (memory B) to make the second memory (memory B) a slave memory.
2. The system of claim 1, wherein the processor (125) further comprises:
  - a trouble monitor (130); and
  - a read/write circuit (140);5 the trouble monitor (130) monitoring the read/write circuit (140) to check for a memory device full indication from the master memory.
3. The system of claim 1, further comprising:
  - a hub (150) in communication with the bus (160) to provide application data to the processor (125).
4. A modular master-slave memory system, comprising:
  - a controller module (100) in communication with a master memory (memory A) and a slave memory (memory B) through first and second independent data paths,  
5 respectively; and
  - an application module (165) in communication the controller module (100);

wherein the application module (165) sends application data to the controller module (100) and the  
10 controller module (100) sends the application data first to the master memory (memory A) and then sends the application data to the slave memory (memory B).

5. The system of claim 4, wherein said controller module (100) is programmed to check the memory capacity of said master and slave memories (memories A & B).

6. The system of claim 4, further comprising:  
a memory module (600) in communication with the controller module (100) to house the master memory (memory A) and a slave memory (memory B).

5

7. The system of claim 4, further comprising:  
a user interface (115) on the controller module (100).

8. The system of claim 7, wherein said controller module (100) is programmed to, in response to said master memory (memory A) having a smaller memory capacity than said slave memory (memory B), send a warning to said user  
5 interface (115) that said master memory (memory A) is too small.

9. The system of claim 8, wherein the controller module (100) is programmed to, in response to said master memory (memory A) having a smaller memory capacity than said slave memory (memory B), reassign memory designations so  
5 that the memory with the smallest memory capacity is the master memory.

10. A method for distinguishing between existing and new memories, comprising:

receiving a first current memory ID representing a first memory (memory A);

receiving a second current memory ID representing a second memory (memory B);

comparing each of the first and second current memory IDs to previously saved respective first and second memory IDs to determine which current memory ID represents an existing memory and which represents a new memory.





Application No: GB0407595.8

Claims searched: 1 - 9

17

Examiner: Michael Powell Waters

Date of search: 13 August 2004

## Patents Act 1977: Search Report under Section 17

### Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
X	1 and 4	US 2002/0051375 A1 (KIM et al) see whole document
X	1 and 4	EP1339212 A2 (CREO) see paragraphs [0057] et seq
X	1 and 4	EP1152428 A2 (SMARTDISK) see figures 1-3 and paragraph [0046] et seq

### Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

### Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC<sup>w</sup> :

G4A

Worldwide search of patent documents classified in the following areas of the IPC<sup>07</sup>

G06F; H04N

The following online and other databases have been used in the preparation of this search report

WPI, EPODOC, PAJ